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Express Mail Label No. EK830777855US

UTILITY PATENT APPLICATION TRANSMITTAL

(Large Entity)

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Docket No. POU9-2000-0047-US1

JC841 U.S. PTO 09/656541 09/06/00

TO THE ASSISTANT COMMISSIONER FOR PATENTS

Box Patent Application

Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.R.F. 1.53(b) is a new utility patent application for an invention entitled:

High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors With A Method To Allow High Speed Bulk Read/Write Operation Synchronous DRAM While Refreshing The Memory

and invented by:

William F. BEAUSOLEIL, R. Bryan COOK, Tak-kwong NG, Helmut ROTH, Peter TANNENBAUM, Lawrence A. THOMAS, and Norton J. TOMASSETTI

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information*:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 13 pages and including the following:

a. ☒ Descriptive Title of the Invention

b. ☒ Cross References to Related Applications (*if applicable*)

c. ☐ Statement Regarding Federally-sponsored Research/Development (*if applicable*)

d. ☐ Reference to Microfiche Appendix (*if applicable*)

e. ☒ Background of the Invention

f. ☒ Brief Summary of the Invention

g. ☒ Brief Description of the Drawings (*if drawings filed*)

h. ☒ Detailed Description

i. ☒ Claim(s) as Classified Below

j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity) (Only for new nonprovisional applications under 37 C.F.R. 1.53(b))	Docket No. POU9-2000-0047-US1

Application Elements (Continued)

3. ☒ Drawing(s) (*when necessary as prescribed by 35 USC 113*)

a. ☐ Formal Number of Sheets _____

b. ☒ Informal Number of Sheets 2

4. ☒ Oath or Declaration

a. ☒ Newly executed (*original or copy*) ☐ Unexecuted

b. ☐ Copy from a prior application (37 CRF 1.63(d)) (*for continuation/divisional application only*)

c. ☐ With Power of Attorney ☐ Without Power of Attorney

d. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference (*usable if Box 4b is checked*)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated herein by reference therein.

6. ☐ Computer Program in Microfiche (*Appendix*)

7. ☐ Nucleotide and/or Amino Acid Sequence Submission (*if applicable, all must be included*)

a. ☐ Paper Copy

b. ☐ Computer Readable Copy (*identical to computer copy*)

c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers (*cover sheet & document(s)*)

9. ☐ 37 CFR 3.73(B) Statement (*when there is an assignee*)

10. ☐ English Translation Document (*if applicable*)

11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS Citations

12. ☐ Preliminary Amendment

13. ☒ Acknowledgment Postcard

14. ☒ Certificate of Mailing

☐ First Class ☒ Express Mail (*Specify Label No.*): EK830777855US

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity) (Only for new nonprovisional applications under 37 C.F.R. 1.53(b))	Docket No. POU9-2000-0047-US1

Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) (*if foreign priority is claimed*)

16. ☐ Additional Enclosures (*please identify below*):

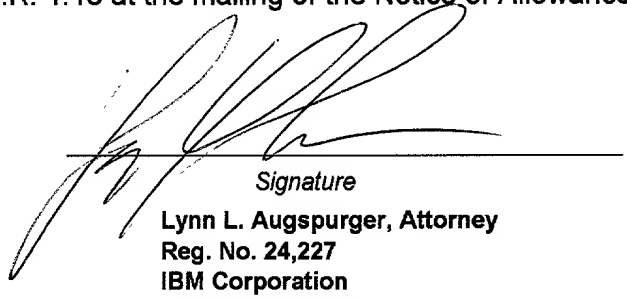
Fee Calculation and Transmittal

CLAIMS AS FILED					
FOR	**#FILED**	**#ALLOWED**	**#EXTRA**	**RATE**	**FEE**
Total Claims	6	- 20 =	0	x $18.00	$0.00
Indep. Claims	2	- 3 =	0	x $ 78.00	$0.00
Multiple Dependent Claims (check if applicable) ☐					$0.00
				BASIC FEE	$690.00
OTHER FEE (*specify purpose*) _____					
				TOTAL FILING FEE	$690.00

☐ A check in the amount of to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **09-0463** as described below. A duplicate copy of this sheet is enclosed.

- ☒ Charge the amount of $690.00 as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.31(b).



Signature

Dated: September 6, 2000

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Docket Number: POU9-2000-0047-US1

HIGH SPEED SOFTWARE DRIVEN EMULATOR COMPRISED OF A PLURALITY OF EMULATION PROCESSORS WITH A METHOD TO ALLOW HIGH SPEED BULK READ/WRITE OPERATION SYNCHRONOUS DRAM WHILE REFRESHING THE MEMORY

APPLICATION FOR

UNITED STATES LETTERS PATENT

"Express Mail" Mailing Label No.: EK830777855US

Date of Deposit: September 6, 2000

I hereby certify that this paper is being deposited with the United States Postal Service as "Express Mail Post Office to Addressee" service under 37 CRF 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

Name: Billy R. Stacy

Signature: Billy R. Stacy

Billy R. Stacy

INTERNATIONAL BUSINESS MACHINES CORPORATION

Title: HIGH SPEED SOFTWARE DRIVEN EMULATOR COMPRISED OF A PLURALITY OF EMULATION PROCESSORS WITH A METHOD TO ALLOW HIGH SPEED BULK READ/WRITE OPERATION SYNCHRONOUS DRAM WHILE REFRESHING THE MEMORY

Cross Reference to Related Applications

The following copending applications, assigned to the assignee of the present invention, contain common disclosure and are incorporated herein by reference in their entireties:

"High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors with Improved Board-to-Board Interconnection Cable Length Identification System," Serial No. _____, filed _____, (Attorney Docket No. POU9-2000-0045-US1).

"High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors with an Improved Maintenance Bus that Streams Data at High Speed," Serial No. _____, filed _____, (Attorney Docket No. POU9-2000-0046-US1).

"High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors with a Method to Allow Memory Read/Writes Without Interrupting the Emulation," Serial No. _____, filed _____, (Attorney Docket No. POU9-2000-0048-US1).

"High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors with Improved Multiplexed Data Memory," Serial No. _____, filed _____, (Attorney Docket No. POU9-1999-0183-US1).

Field of the Invention:

This invention relates to a software driven emulator comprised of a large number of single bit processors operating in parallel to execute, at high speed, an emulation of a complex processor, and more particularly, to a system and method for high-speed streaming of bulk read and write operations from and to the synchronous DRAM module memories in order to support a simulation-accelerate mode of operation.

Trademarks:

Background:

The usefulness of software driven emulators has increased enormously with growth in the complexity of integrated circuits. Basically, an emulation engine operates to mimic the logical design of a set of one or more integrated circuit chips. The emulation of these chips in terms of their logical design is highly desirable for several reasons. The utilization of emulation engines has also grown up with and around the corresponding utilization of design automation tools for the construction and design of integrated circuit chip devices. In particular, as part of the input for the design automation process, logic descriptions of the desired circuit chip functions

are provided. The existence of such software tools for processing these descriptions in the design process is well suited to the utilization of emulation engines which are electrically configured to duplicate the same logic function that is provided by a design automation tool.

Utilization of emulation devices permits testing and verification via electrical circuits of logic designs before these designs are committed to a socalled "silicon foundry" for manufacture. The input to such foundries is the functional logic description required for the chip and its output is initially a set of photolithographic masks which are then used in the manufacture of the desired electrical circuit chip device. Verifying that logic designs are correct in the early stage of chip manufacturing eliminates the need for costly and timeconsuming second passes through a silicon foundry.

Another advantage of emulation systems is that they provide a device that makes possible the early validation of software meant to operate the emulated chips. Thus, software can be designed, evaluated and tested well before the time when actual circuit chips become available. Additionally, emulation systems can also operate as simulator-accelerator devices thus providing a highspeed simulation platform.

Emulation engines of the type contemplated by this invention contain an interconnected array of emulation processors (EP). Each emulation processor (hereinafter, also sometimes simply referred to as "processor") can be programmed to evaluate logic function (for example, AND, OR, XOR, NOT, NOR, NAND, etc.). The program driven processors operate together as an interconnected unit, emulate the entire desired logic design. However, as integrated circuit designs grow in size, more emulation

processors are required to accomplish the emulation task. An aim, therefore, is to increase the capacity of emulation engines in order to meet the increasingly difficult task of emulating more and more complex circuits and logic functions by increasing the number of emulation processors in each of its modules.

For purposes of better understanding the structure and operation of emulation devices generally, and this invention particularly, United States Patent No. 5,551,013 and patent application Serial No. 09/373,125 filed August 12, 1999, both of which are assigned to the assignee of this application, are hereby incorporated herein by reference.

Patent No. 5,551,013 shows an emulation chip, called a module here, having multiple (e.g. 64) processors. All processors within the module are identical. The sequencer and the interconnection network occurs only once in a module. The control stores hold a program created by an emulation compiler for a specified processor. The stacks hold data and inputs previously generated and are addressed by fields in a corresponding control word to locate the bits for input to the logic element. During each step of the sequencer an emulation processor emulates a logic function according to the emulation program. A data flow control interprets the current control word to route and latch data within the processor. The node-bit-out signal from a specified processor is presented to the interconnection network where it is distributed to each of the multiplexors (one for each processor) of the module. The node address field in the control word allows a specified processor to select for its node-bit-in signal the node-bit-out signal from any of the processors within its module. The node bit is stored in the input stack on every step. During any operation the

node-bit-out signal of a specified processor may be accessed by none, one, or all of the processors within the module.

Data routing within each processor's data flow and through the interconnection network occurs independently of and overlaps the execution of the logic emulation function in each processor. Each control store stores control words executed sequentially under control of the sequencer and program steps in the associated module. Each revolution of the sequencer causes the step value to advance from zero to a predetermined maximum value and corresponds to one target clock cycle for the emulated design. A control word in the control store is simultaneously selected during each step of the sequencer. A logic function operation is defined by each control word.

Each of these emulation processors has an execution unit for processing multiple types of logic gate functions. Each emulation processor switches from a specified one logic gate function to a next logic gate function in a switched-emulation sequence of different gate functions. The switched-emulation sequence of each of the processors thus can emulate a subset of gates in a hardware arrangement in which gates are of any type that the emulation processors functionally represent for a sequence of clock cycles. The processors are coupled by a like number of multiplexors having outputs respectively connected to the emulation processors of a module and having inputs respectively connected to each of the other emulation processors. The bus connected to the multiplexors enables an output from any emulation processor to be transferred to an input of any other of the emulation processors. In accordance with the teachings of the pending application, the basic design of the 5,551,013 patent is improved by interconnecting processors into clusters. With interconnected clusters, the evaluation phases can be cascaded

and all processors in a cluster perform the setup and storing of results in parallel. This setup includes routing of the data through multiple evaluation units for the evaluation phase. For most efficient operation, the input stack and data stack of each processor must be stored in shared memory within each cluster. Then, all processors perform the storage phase, again in parallel. The net result is multiple cascaded evaluations performed in a single emulation step. Every processor in a cluster can access the input and data stacks of every other processor in the cluster and less space on each module chip for the functions that support the processor operation, particularly the memory functions.

As will be appreciated by those skilled in the art, emulators of the type described above have evolved to perform not only in a traditional emulation mode but also in a simulation-accelerate mode. In this simulation-accelerate mode, there is a requirement to upload and download large quantities of data from the system SDRAMs for the data capture function of the simulation-accelerate operating mode.

In the prior art emulators, such as the ET 3.5 and ET 3.7 emulators, the protocol for writing data to and reading data from SDRAMS requires a hand shake protocol. A word is transferred from or to the SDRAM only in response to a "done" signal from the memory signaling that the previous transfer operation has been completed. The "done" signal is required in these prior art systems to account for the case where the previous transfer operation was delayed by a memory refresh operation. Such prior art protocols slow the bulk transfer of data to and from an SDRAM memory.

Summary of the Invention:

An object of this invention is the provision of a system and method for rapidly transferring large quantities of data to and from SDRAM memories in an emulator in order to support simulation-acceleration operating mode.

Briefly, this invention contemplates the provision of a system and method for bulk transfer to and from the SRAMs in which a starting memory address is latched and is then incremented every clock cycle to generate a new memory address, as described more extensively in copending application Serial No. _____, filed _____ (POU9-2000-0048-US1) and assigned to the assignee of this application. The addresses are decoded and memory requests are pipelined to the SRAM memory, one every clock cycle. When the memory controller detects transfer of the boundary of a predetermined number of clock cycles or words (e.g. 64 words or four clock cycles) the burst mode of data transfer is stopped and the memory controller waits for a "done" signal before resuming another cycle of the burst transfer mode. The memory controller on detecting a request on this address boundary first does a memory refresh followed by a requested operation; e.g. a continuation of the transfer operation.

Brief Description of the Drawings:

The foregoing and other features and advantages of the invention will be described with reference to the accompanying drawings. In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. Also in the figures, the left most digit of each reference number corresponds to the figure in which the reference number is first used.

Figure 1 is a high level block diagram of two of 64 modules on an emulator board of the type to which this invention is applicable.

Figure 2 is a flow diagram of the method steps of this invention.

Detailed Description of the Invention:

Referring now to Figure 1, each board 14 of the emulation processor in this exemplary embodiment has sixty-four modules 12, two of which are illustrated in Figure 1. Each module has an E4 chip 16, which includes sixty-four single-bit processors. Each module has a main memory 18 comprised of two SDRAMs and a single SSRAM. These memories communicate internally with the E4 chip 16 on the module to which these memories are attached, via an internal module bus. A maintenance bus connects these module main memories to other modules on the same board, to modules on other boards, and to a work station 26, which serves the entire emulation engine. There is one memory controller 22 for each board. The memory controller 22 interfaces the reading and writing of data from and into the SDRAMs and SSRAMs in a data capture mode of operation in which bulk transfers of data between the work station and the SDRAMs and SSRAMs are carried out via the maintenance bus.

For bulk transfers in accordance with the teachings of this invention, a latch is set by one of the ET4 control stores to inhibit further transfers between the ET4 processor chip and the SDRAMs on the module, as described in detail in copending application serial number _____, (POU9-2000-0048-US1). The memory controller 22 includes incrementing logic into which a starting SDRAM address is inserted when the emulator is to perform a bulk data transfer operation. This memory address in incremented by "1" in response to each clock signal. Similarly,

with the latch set, the memory controller makes a memory request (i.e. read or write) to the incremented address in response every clock cycle. Periodically, the memory controller, after making a memory request, waits for the memory "done" return before making the next memory request. This periodic pause in the streamed bulk memory transfer allows time for the SDRAM refresh cycle, the completion of which is signaled by the "done" return signal. As will be appreciated by those skilled in the art, the minimum frequency at which there is a pause in the bulk streaming operation is a function of the frequency at which the SDRAM must be refreshed. In one specific example, an emulator of the type described herein uses commercially available SRAMs, has a clock cycle of 90 ns, and transfers data to and from the SDRAM on each clock cycle as a sixteen-bit word for each memory address. The memory controller detects each 64 word boundary and stops the burst mode of data transfer while the controller waits for a "done" return from the memory in order to resume the burst mode. Upon detecting the 64 word boundary, the memory controller initiates a refresh cycle.

Referring now to Figure 2 of the drawings, in a bulk data transfer to the module memories, a latch is set (block 30) and a starting address is entered into a register of the memory controller (block 32). A sixteen bit data word is transferred each clock cycle (block 34) the address is incremented (block 36) and another word is transferred to or from this incremented address on the next clock cycle (block 37). After a predetermined number of clock cycles or on a predetermined word boundary (e.g. on each 64 word boundary) (block 38) the bulk transfer is halted while the memory controller waits for a "done" return (block 40). When the "done" (block 39) signal is returned, the controller resumes the streaming mode of operation, which continues until the next 64 word boundary is detected.

While the preferred embodiment to the invention has been described, it will be understood that those skilled in the art, both now and in the future, may make various improvements and enhancements which fall within the scope of the claims which follow. These claims should be construed to maintain the proper protection for the invention first described.

What is claimed is:

Claim 1. In a software driven emulator comprised of a plurality of modules on printed circuit boards, each of said modules including a processor chip and at least one SDRAM coupled to the processor chip, a maintenance bus coupled to said SDRAM, and a memory controller coupled to said maintenance bus, a method executing bulk data transfers to said SDRAM via said maintenance bus, including the steps of:

transferring data to said SDRAM via said maintenance bus on each clock cycle for a predetermined number of clock cycles in succession;

halting the transfer of data after said predetermined number of data transfers;

initiating a SDRAM refresh cycle after said halting step;

resuming said transferring step upon receipt of a done signal after said refresh cycle.

Claim 2. In a software driven emulator comprised of a plurality of modules on printed circuit boards, each of said modules including a processor chip and at least one SDRAM coupled to the processor chip, a maintenance bus coupled to said SDRAM, and a memory controller coupled to said maintenance bus, a method executing bulk data transfers to said SDRAM via said maintenance bus, including the steps of:

transferring data from said SDRAM via said maintenance bus on each clock cycle for a predetermined number of clock cycles in succession;

halting the transfer of data after said predetermined number of data transfers;

initiating a SDRAM refresh cycle after said halting step;

resuming said transferring step upon receipt of a done signal after said refresh cycle.

Claim 3. A method of executing bulk transfers as in claim 1 including establishing a starting address for said bulk transfer in said memory controller and incrementing said starting address by one on each clock cycle.

Claim 4. A method of executing bulk transfers as in claim 2 including establishing a starting address for said bulk transfer in said memory controller and incrementing said starting address by one on each clock cycle.

Claim 5. A method of executing bulk transfers as in claim 1 wherein a data word is transferred on each clock cycle.

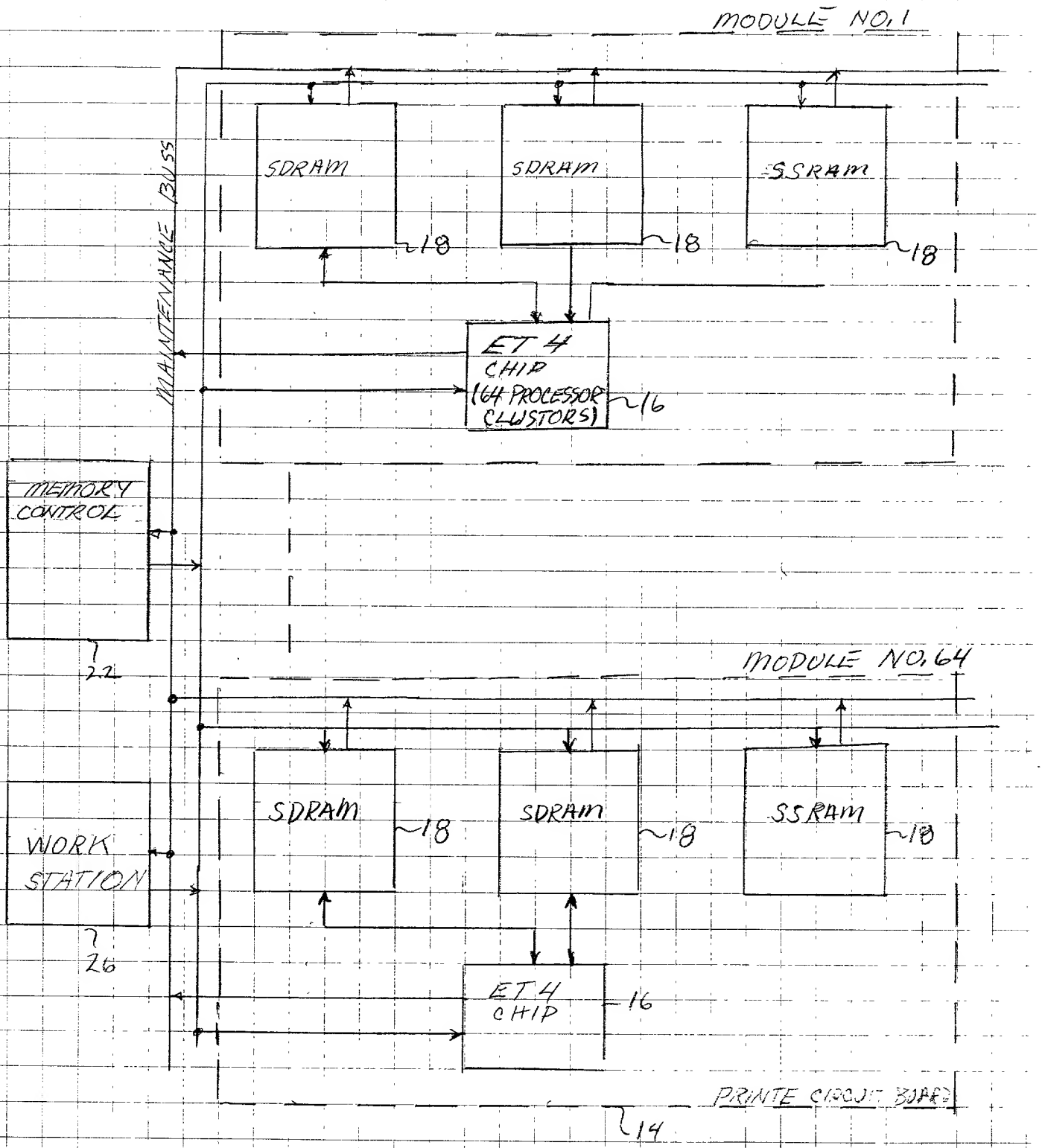
Claim 6. A method of executing bulk transfers as in claim 2 wherein a data word is transferred on each clock cycle.

Title: HIGH SPEED SOFTWARE DRIVEN EMULATOR COMPRISED OF A PLURALITY OF EMULATION PROCESSORS WITH A METHOD TO ALLOW HIGH SPEED BULK READ/WRITE OPERATION SYNCHRONOUS DRAM WHILE REFRESHING THE MEMORY

Abstract of the Disclosure:

A system and method for bulk transfer to and from the SRAMs in which a starting memory address is latched and is then incremented every clock cycle to generate a new memory address. The addresses are decoded and memory requests are pipelined to the SRAM memory, one every clock cycle. When the memory controller detects transfer of the boundary of a predetermined number of clock cycles or words (e.g. 64 words or four clock cycles) the burst mode of data transfer is stopped and the memory controller waits for a "done" signal before resuming another cycle of the burst transfer mode. The memory controller on detecting a request on this address boundary first does a memory refresh followed by a requested operation; e.g. a continuation of the transfer operation.

FIG 1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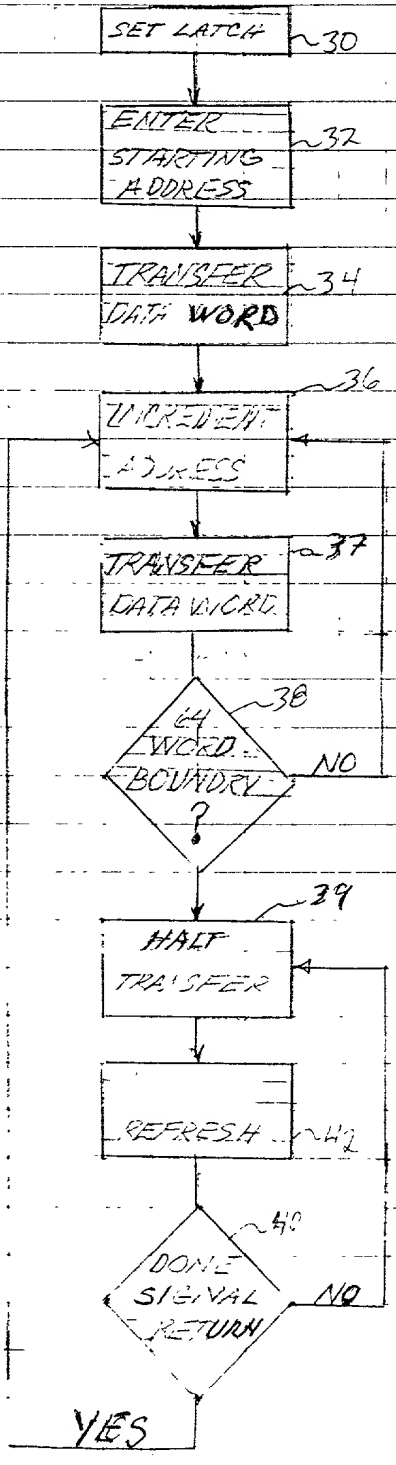
SDRAM
18
SDRAM
18
SSRAM
18
MAINTENANCE BUSS
ET 4
CHIP
(64 PROCESSOR
CLUSTORS)
16
MEMORY
CONTROL
22
MODULE NO. 64
SDRAM
18
SDRAM
18
SSRAM
18
WORK
STATION
26
ET 4
CHIP
16
PRINTE CIRCUIT BOARD
14

FIG 2


SET LATCH
30
ENTER STARTING ADDRESS
32
TRANSFER DATA WORD
34
36
INCREMENT ADDRESS
TRANSFER DATA W.CRD.
37
64 WORD BOUNDRY ?
38
NO
39
HALT TRANSFER
REFRESH
42
40
DONE SIGNAL RETURN
NO
YES

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **HIGH SPEED SOFTWARE DRIVEN EMULATOR COMPRISED OF A PLURALITY OF EMULATION PROCESSORS WITH A METHOD TO ALLOW HIGH SPEED BULK READ/WRITE OPERATION SYNCHRONOUS DRAM WHILE REFRESHING THE MEMORY**

the specification of which (check one)

_X_ is attached hereto
___ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including claims, as amended by any amendment referred to above. I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR Section 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

			Priority Claimed
(Number)	(Country)	(Day/Month/Year Filed)	__ Yes __ No
(Number)	(Country)	(Day/Month/Year Filed)	__ Yes __ No

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below.

(Application Number) (Filing Date)

(Application Number) (Filing Date)

I hereby claim the benefit under 35 U.S.C Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose material information as defined in 37 CFR Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Appl. Serial No.)	(Filing Date)	(Status)(patented, pending, abandoned)
(Appl. Serial No.)	(Filing Date)	(Status)(patented, pending, abandoned)

ADDED PAGE TO COMBINED DECLARATION AND POWER OF ATTORNEY FOR SIGNATURE BY FIRST AND SUBSEQUENT INVENTORS

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Signature: R Bryan Cook Date: 9/5/2000

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Post Office Address: Same as above

Full Name of third joint inventor: Tak-kwong NG

Signature: Tak Kwong Ng Date: 8/31/2000

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Citizenship: United States

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Post Office Address: Same as above

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Signature: Lawrence A. Thomas Date: 9/1/2000

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Citizenship: United States

Post Office Address: Same as above

Full Name of seventh joint inventor: Norton J. TOMASSETTI

Signature: Norton J. Tomassetti Date: 9/1/2000

Residence: 169 Parsell Street, Kingston, New York 12401

Citizenship: United States

Post Office Address: Same as above